(54) PWM control apparatus

(57)   A pulse Width Modulation (PWM) control circuit
(10) is used in a switched-mode power supply (SMPS)
(5) having a normal mode and a standby mode, for con-
trolling and regulating the SMPS. An input of the PWM
control circuit (10) is arranged to receive a signal indi-
cating an amount of current supplied by the supply. An
over-current determining arrangement provides an
over-current signal in the event of there being an over-
current condition in the signal indicating the amount of
current supplied by the supply. A further input (3) of the
PWM control circuit receives a regulation signal in the
event of there being a regulation output from circuitry
coupled to receive power from the SMPS. A logic circuit
within the PWM control circuit compares the over-cur-
rent signal and the regulation signal in order to deter-
mine whether the switched-mode power supply is in
standby mode or normal mode, thus avoiding the need
for a dedicated control pin to indicate standby and nor-
mal modes.

FIG. 1

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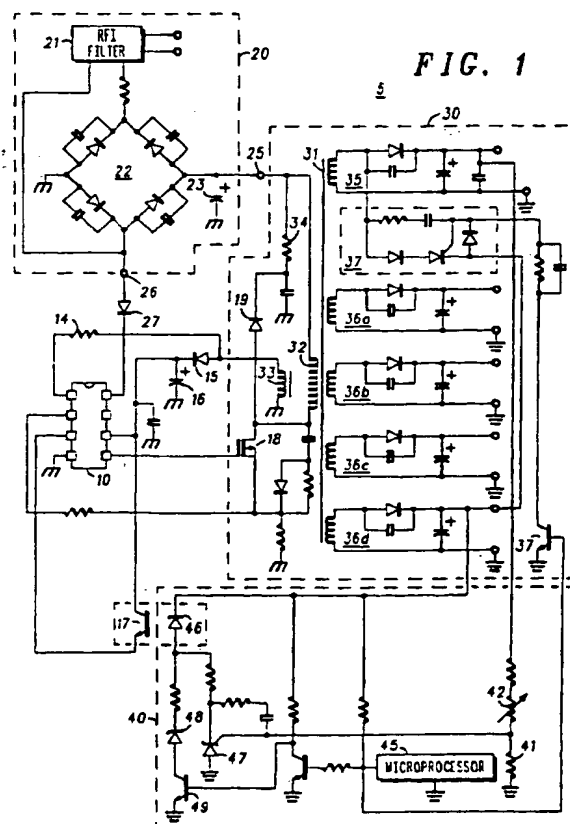
Description

Field of the Invention

[0001] This invention relates to pulse-width modulated control apparatus, and particularly but not exclusively for such apparatus when used to control a switched-mode power supply.

Background of the Invention

[0002] Switched-Mode Power Supplies (SMPS) are being increasingly used in many domestic and industrial applications. In applications such as televisions or computer monitors, the application may require a number of states or modes of operation. A first 'off' mode occurs when there is no power supplied to a device (or when a master switch is off); a second 'on' mode occurs when the device is switched on an operating normally; and a third mode (referred to as a standby mode) occurs when the device is to remain powered, but with reduced functions and reduced power consumption. A standby mode may be encountered in a television via an 'off' switch of a remote control, which typically does not switch the television fully off, but allows certain circuitry within the television to remain powered, so that if the 'on' button of the remote control is pressed, the television will return to the 'on' mode.

[0003] There is a need to reduce the power consumed by the SMPS during standby mode, so that use of mains electricity is reduced. At present there is a goal to reduce the power consumption during standby mode to a value of the order of 1 Watt.

[0004] Burst mode SMPS are known, which have an efficient power consumption in standby mode. However the PWM control apparatus are not easy to implement for burst-mode SNIPS, they generate much noise due to the 'burst' nature of their operation, and they require a large number of connections and external components, leading to a semiconductor package having many connection pins, and a large printed circuit board with many components.

[0005] Therefore what is needed is PWM control apparatus for SMPS with a reduced number of discrete components, a reduced pin count and size, and low power consumption in standby mode.

[0006] This invention seeks to provide a power supply which mitigates the above mentioned disadvantages.

Summary of the Invention

[0007] According to the present invention there is provided a PWM control apparatus as claimed in claim 1.

[0008] In this way a PWM control apparatus for a SMPS is provided with a reduced number of discrete components, a reduced pin count and size, and low power consumption in standby mode.

Brief Description of the Drawing(s)

[0009] An exemplary embodiment of the invention will now be described with reference to the drawing in which:

FIG. 1 shows a preferred embodiment of a switched-mode power supply in accordance with the invention;

FIG. 2 shows a block diagram of a PWM control circuit forming part of the switched-mode power supply of FIG. 1;

FIG. 3 shows a graph illustrating operating phases of the PWM control circuit of FIG. 2;

FIG. 4 shows an illustrative block diagram of two functions combined in a single pin of the PWM control circuit of FIG. 2; and

FIG. 5 shows an illustrative block diagram of a mode selection function using two pins of the PWM control circuit of FIG. 2.

Detailed Description of a Preferred Embodiment

[0010] Referring to FIG. 1, there is shown a switched-mode power supply arrangement (SMPS) 5, as might be found in a domestic appliance requiring a high-voltage supply, such as a television. A typical domestic appliance of this nature may include the feature of a standby mode of operation, whereby the appliance remains switched on, but with reduced functionality and reduced power consumption. The SMPS arrangement 5 includes a PWM control circuit 10, a mains supply arrangement 20, a transformer arrangement 30 and a microprocessor and regulation arrangement 40.

[0011] The PWM control circuit 10, which will be further described with reference to FIG.2 below, is integrated as a semiconductor package having 8 connection pins.

[0012] The mains supply arrangement comprises a filter 21, a diode bridge 22 and a bulk capacitor 23 arranged to provide a rectified signal to a node 25. A further node 26 provides a signal directly from the filter 21 to pin 8 of the PWM control circuit 10, via a diode 27.

[0013] The transformer arrangement 30 has a magnetic core 31, and a primary winding 32 and an auxiliary winding 33 arranged on one side of the core. The primary winding 32 has one node coupled to the node 25, and a further node coupled to a clamping transistor 18 to be further described below. The auxiliary winding has one node coupled to ground and a further node coupled to pins 1 and 6 of PWM control circuit 10 via a resistor 14, and diode 15 with storage capacitor 16 respectively.

[0014] A high-voltage secondary winding 35 and low-voltage secondary windings 36a, b, c and d are arranged on the other side of the core. The high voltage

winding 35 is arranged to provide a high voltage supply (~100V) to appropriate high voltage components of the appliance (not shown) during normal mode of operation. The low voltage windings 36a, b, c and d are arranged to provide low voltage supplies (~10V) to various low voltage components of the appliance. Secondary winding 36d is coupled to provide a low voltage supply for the microprocessor and regulation arrangement 40, which is also provided for regulation purposes, to be further described below.

[0015] The microprocessor and regulation arrangement 40 has a microprocessor 45 arranged to control the management of the standby mode (and normal mode) of operation of the SMPS, in addition to other functions (not shown). When the power supplied to the secondary side of the transformer arrangement 30 has reached the desired level, regulation is achieved via in optocoupler arrangement in series with a regulating diode 47.

[0016] The breakdown voltage of the regulating diode 47 is adjustable via a potential divider circuit of resistor 41 and output level variable resistor 42, coupled to the output of the high voltage winding 35. In this way the regulating diode conducts a current according to the voltage obtained by the resistor divider arrangement of resistor 41 and output level variable resistor 42. This current flows through a Light Emitting Diode (LED) 46 of the optocoupler arrangement, inducing a signal in a photovoltaic cell 17 thereof. The photovoltaic cell is coupled between the storage capacitor 16 and pin 3 of the PWM control circuit 10.

[0017] When the PWM control circuit 10 receives a regulation signal from the photovoltaic cell 17 via pin 3, a signal is from pin 5 of the circuit 10 turns on a clamping transistor 18, which clamps both nodes of the primary winding 32 to the node 25, vi a clamping network of diode 19 and resistor 34. In this way the clamping transistor 18 acts as a power switch.

[0018] When the appliance switches to standby mode, the high voltage components of the appliance no longer require power. The microprocessor 45 reconfigures the secondary windings of the transformer arrangement 30 by turning on a transistor 37 which effectively clamps the high voltage winding 35 to a rectified voltage of the secondary winding 36d via the diode arrangement 37. The microprocessor also turns on a transistor 49, which effectively inserts a second zener diode 48 into the path of the LED 46, thus providing a means of regulation in standby mode, the rectified voltage of secondary winding 36d being forced riot to exceed the sum of: the breakdown value of the regulating diode 47 plus the voltage drop across the LED 46 and the transistor 49.

[0019] Referring now also to FIG. 2, there is shown a block diagram of the PWM control circuit 10. Essentially, three control pins, pins 1, 2 and 3 provide inputs for all of the required variable signals used to control the SMPS. Pin 1 accommodates a zero current detection input and a negative voltage clamp. Pin 2 combines

over-current protection with a standby peak current limit value. Pin 3 combines the current sense voltage (regulation) input with standby regulation.

[0020] The remaining pins provide supply and output connections: Pin 4 is coupled to ground, pin 5 drives the power switch arrangement of clamping transistor 18, pin 6 is coupled to the auxiliary winding 33 via the storage capacitor 16 (Vcc), and pin 8 is coupled to node 26 of the mains supply arrangement 20 (high voltage). Pin 7 is left unconnected, in order to improve isolation between pins 8 (high voltage) and 6 (Vcc).

[0021] Regulation is provided in the following way. The control block 130 is coupled to receive the regulation signal from pin 3. This is used to inform the drive control block 150, via the PWM control block 140, of the desired duty cycle of the output, which is then used to drive the output buffer 190 accordingly to control the power switch arrangement of clamping transistor 18.

[0022] Standby mode and normal mode are detected by the standby management block, which takes inputs from the demagnetisation block 110 (pin 1), the current sense block 120 (pin 2), and from the control block 130 (pin 3 via the drive control block 150). The mode detection is to be further described below with reference to FIG. 5.

[0023] When standby mode commences, the microprocessor 45 reconfigures the secondary side of the transformer arrangement 30 as described above. Due to the reconfiguration of the transformer arrangement 30 the regulation signal Vpwm will effectively regulate the high-voltage winding 35 to a voltage level in the order of 10V. The voltages of all of the secondary windings will be reduced, which in turn causes the current developed in the auxiliary winding 33 to drop below that required to maintain power to the control circuit 10. At this time power is drained from the bulk capacitor 16 which causes Vcc to fall slowly.

[0024] Referring now also to FIG. 3, there is shown a graph illustrating three operating phases of the PWM control circuit 10, in terms of the behaviour of Vcc during standby mode.

[0025] In a first phase (so-called start-up phase) 215, insufficient current is provided by the auxiliary winding 33 to power the PWM control circuit 10, leading to Vcc being below a second undervoltage level 260, to be further described below (for example when the arrangement is turned on, or in standby mode as described in the preceding paragraph). During this first phase 210, the start-up current source 180 draws current directly from the filter 21 via the node 26 and diode 27, and supplies the current to the storage capacitor 16 which causes Vcc to rise steadily during this phase (line 210) until Vcc reaches a start-up threshold 240 (determined and detected within the Vcc management block 170).

[0026] In a second phase (so-called working phase) 225, the PWM control circuit 10 operates normally, drawing current from Vcc. (if the arrangement is in normal mode, Vcc would stay at or above the first under-

voltage level 250, and the circuit 10 would continue operating normally). In standby mode, Vcc drops due to the insufficient current developed from the auxiliary winding 33 (line 220), until Vcc reaches a first under-voltage level 250.

[0027] In a third phase (so-called latched-off phase) 235, the PWM control circuit 10 is switched off, as is the start-up current source 120. Thus in this third phase, very little current is drawn from Vcc, and Vcc therefore falls only very slowly, until it reaches the second under-voltage level 260, whereupon the start-up current source is again turned on, reverting again to the first phase 215.

[0028] The first, second and third phases 215, 225 and 235 respectively, are controlled by the Vcc management block 170, which produces signals indicating the phases as they occur.

[0029] Referring now also to FIG. 4, there is shown an illustrative block diagram of an over-current limit function of the PWM control circuit 10. Pin 2 is coupled to a non-inverting input of a comparator 320, and to a current source 310 via a switch 315. An inverting input of the comparator 320 is arranged to receive an over-current protection threshold voltage. In this way, should the voltage at pin 2 exceed the threshold voltage, the output of the comparator will generate a signal, indicating an over-current condition.

[0030] Pin 2 is further coupled via a first resistor 340 to a point of divided potential 345. The point of divided potential 345 is coupled between the primary winding 32 via the power switch (clamping transistor 18), and ground via second resistor 350.

[0031] The switch 315 is switched in dependence upon the output of an AND gate 330, which is coupled to receive standby and working phase input signals. Therefore, in the event that the circuit 10 is in standby mode, the current source 310 is switched to be coupled to pin 2, thereby introducing a further current source to drain current via the second resistor 350 and the first resistor 340, thereby raising the voltage at pin 2. In this way, during standby mode, the over-current protection threshold is effectively reduced (by artificially raising the voltage at pin 2) and may be programmed by the value of the first resistor 340. The first resistor 340 may be partially or totally integrated with the PWM control circuit 10.

[0032] Referring now also to FIG. 5, there is shown a latch arrangement 400 forming part of the standby block, and having first and second latches 410 and 440 respectively, and first and second AND gates 420 and 430 respectively.

[0033] The first latch 410 is set by an over-current signal derived from the Current sense block 120, and reset by a regulation signal (Rpwm) derived from the control block 130 and the PWM control block 140. Rpwm is a pulse signal which terminates the supply of power during normal mode steady-state.

[0034] The value of the first latch 410 is clocked to the first AND gate 420, which also receives a start-up phase signal from the Vcc management block 170.

[0035] The inverted value of the first latch 410 is clocked to the second AND gate 430, which also receives a latched-off phase signal from the Vcc management block 170.

[0036] The second latch 440 is set by an output of the second AND gate 430, and reset by an output of the first AND gate 420.

[0037] The determination of standby mode is performed in the following way. A latched-off phase 235 will occur if Vcc decays below the first under-voltage level 250, which is caused by insufficient power developed in the auxiliary winding 33. There are two possible reasons for this:

  a) A fault condition (for example an overload) has occurred, causing the controller 10 to effectively switch off the SMPS.
  b) Standby mode has been entered by the microprocessor 45 as described above.

[0038] In the latter case, a regulation signal will have been received at the end of the working phase 225, due to the excess voltage present at the moment of reconfiguration. Therefore the first latch 410 will have a low value, its inverted output will be high, as will the two inputs to the second AND gate 430, resulting in the second latch 440 being set, thus indicating standby mode.

[0039] Similarly the determination of normal mode is performed in the following way. Assuming that the PWM control circuit 10 is already in standby mode, the current source 310 will be switched on, effectively reducing the voltage threshold level of the comparator 320. Therefore when the microprocessor 45 decides to re-enter normal mode, and reconfigures the secondary windings accordingly, a large amount of current will then be demanded. This will lead to successive on-time terminated by the over-current protection (with an over-current protection signal) and no regulation (therefore no regulation signals) at the end of the switching phase. In this way the first latch 410 will be latched with a high value, and consequently the output of the first AND gate 420 will be high during the next start-up phase. This leads to the second latch 440 being reset, effectively cancelling the standby mode within the PWM control circuit 10, and returning to normal mode.

[0040] It will be appreciated that alternative embodiments to the one described above are possible. For example, this arrangement could be used wwith any type of SMPS, with fixed or variable frequency, and with current or voltage modes. The precise arrangement of the SMPS may differ from that described, Whilst still allowing the PWM control circuit 10 to operate substantially as described.

[0041] The microprocessor and regulation arrangement 40 could differ in implementation from that described. For example, the regulating diode 47 could be

replaced with an operational amplifier.

[0042] Furthermore, the latch arrangement 400 may be replaced by an alternative logic arrangement implementing substantially the same function. For example, the first AND gate 420 could be arranged to receive the latched-off phase signal, and the second AND gate would then receive the start-up signal, with an appropriate change to the operation of the latches.

Claims

1. Pulse Width Modulation control apparatus for use with a switched-mode power supply having a normal mode and a standby mode, comprising:

    a first input arranged to receive a signal indicating an amount of current supplied by the supply; over-current determining cleans coupled to the first input for providing an over-current signal in the event of there being an over-current condition in the signal indicating the amount of current supplied by the supply; a second input arranged to receive a regulation signal in the event of there being a regulation output from circuitry coupled to receive power from the power supply; and, logic means for comparing the over-current signal and the regulation signal in order to determine whether the switched-mode power supply is in standby mode or normal mode.

2. The pulse width modulation control apparatus of claim 1 further comprising means for determining the state of a operating supply voltage to the apparatus, wherein the logic means is further arranged to receive a signal indicating the state of the operating supply voltage, for use in determining whether the switched-mode power supply is in standby mode or normal mode.

3. The pulse width modulation control apparatus of claim 1 or claim 2 wherein the logic means comprises latch means arranged to latch the over-current and regulation signals.

4. The pulse width modulation control apparatus of any preceding claim further including a selectively switchable current source coupled to the first input wherein during standby mode, the switchable current source is switched to increase the voltage at the first input, thereby reducing a threshold level for the over-current condition.

5. The pulse width modulation control apparatus of any preceding claim, having three control pins.

6. The pulse width modulation control apparatus of

claim 5, encapsulated in an 8-pin plastic package.

7. The pulse width modulation control apparatus of claim 6, wherein one pin is provided to improve isolation between two power supply pins.
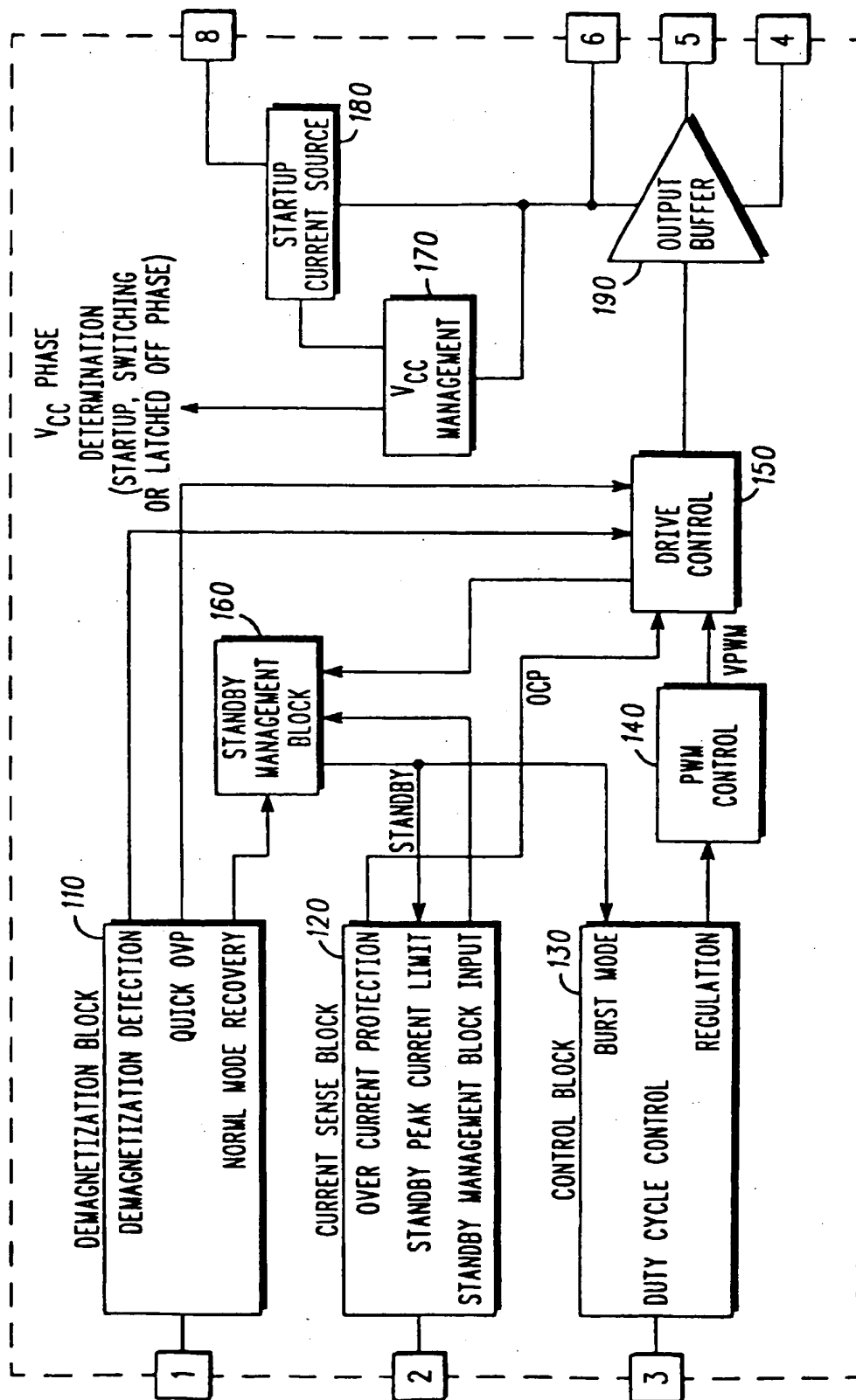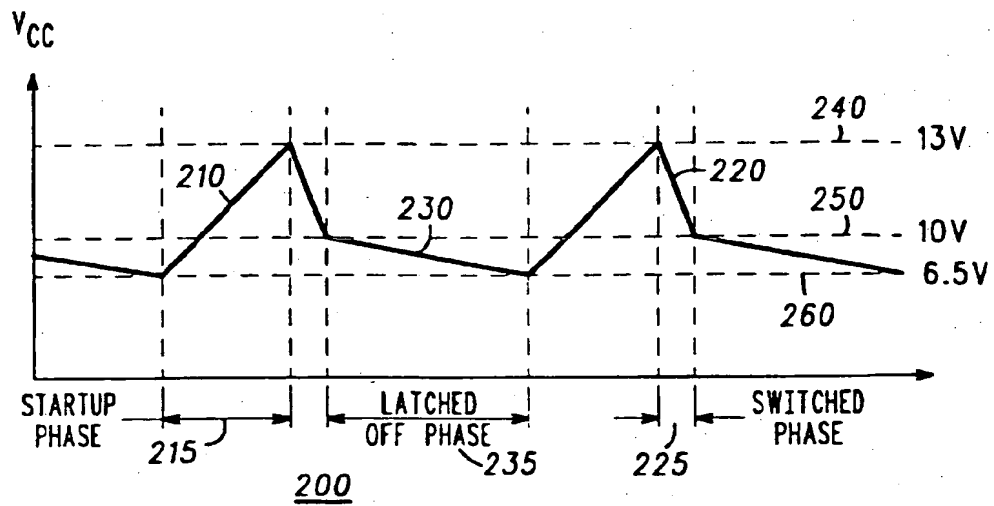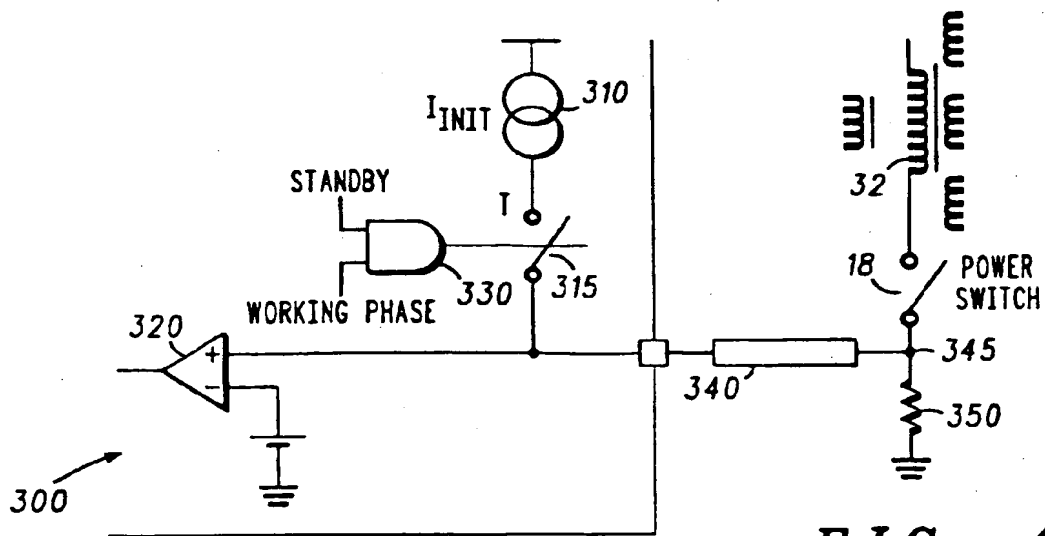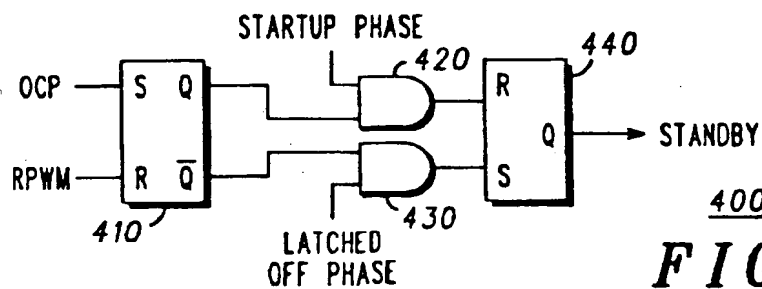
FIG. 1
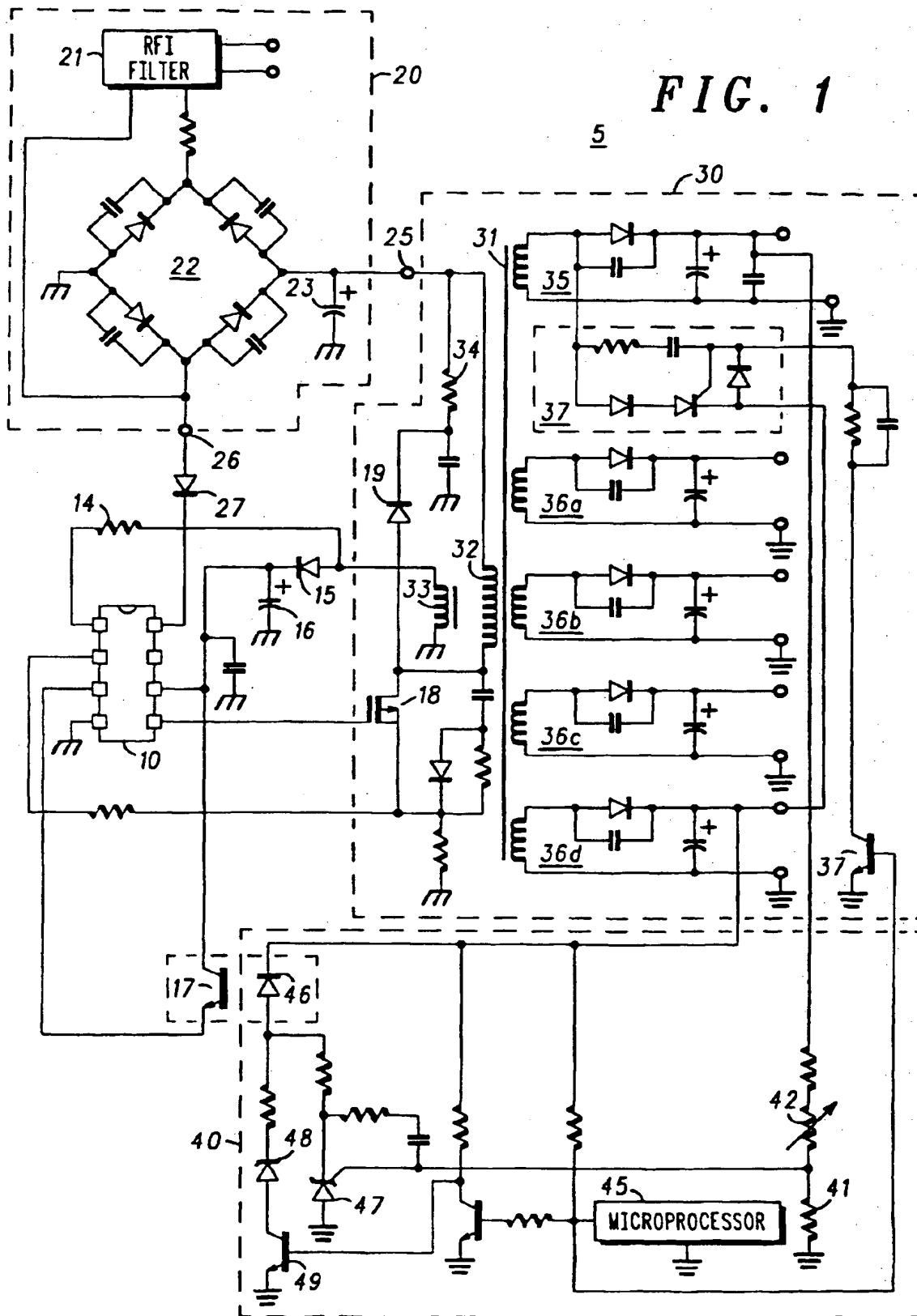
FIG. 2

FIG. 3

FIG. 4

FIG. 5

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 99 40 1317

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 5 812 383 A (MOBERS TOM ET AL) 22 September 1998 (1998-09-22) * the whole document *	1-7	H02M3/335
A	US 5 689 407 A (DE BONDT GUY L P ET AL) 18 November 1997 (1997-11-18) * the whole document *	1-7	
A	PHILIPS SEMICONDUCTORS: "Greenchip SMPS module TEA1566" DATA SHEET,20 April 1999 (1999-04-20), XP002122143 http://www-us2.semiconductors.philips.com/ acrobat/datasheets/TEA1566_N_1.pdf * the whole document *	1-7	
T	MOTOROLA: "Greenline very high voltage PWM controller" DATA SHEET,July 1999 (1999-07), XP002122144 http://scgproducts.motorola.com/Collateral /DataSheet/mc44608rev0.pdf * the whole document *	1-7	

TECHNICAL FIELDS
SEARCHED   (Int.Cl.7)

H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 November 1999	Thisse, S

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EP 99 40 1317

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10-11-1999

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